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$S_i = C_i + A_i + B_i$ ,  $C_{i+1} = C_i(A_i + B_i) + A_i B_i$ .

VLSI Test Principles and Architectures Ch. 2 - Design for Testability - P. 3/12. 2.5 (Ad Hoc Technique) Fig. 7: An example of a combinational feedback loop in a combinational circuit. Figure 7 shows an example of a combinational feedback loop. In this example, when  $A = 1$ ,  $B = 0$ , and  $C = 1$ , the circuit acts as an oscillator, which prevents us from being able to predict a valid value at  $G$ .

## *Chapter 2 Exercise Solutions 2.1 Testability Analysis*

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- Test Compression - P. 1/3. Chapter 6

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*Chapter 6 Exercise Solutions - IC-Test Lab, NCUE, Taiwan*

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